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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/762,517	06/07/2001	Franz Hutner	112740-147	4803

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EXAMINER

WHITTINGTON, ANTHONY T

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 05/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/762,517

Applicant(s)

HUTNER, FRANZ

Examiner

Anthony T Whittington

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 April 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 10-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10-16 and 18 is/are rejected.
- 7) ☒ Claim(s) 17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Allowable Subject Matter

Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 17, the prior art of record neither singularly nor in combination teaches the limitations: “counter for counting a bus clock signal” and “input/output drivers are only selected during all even-numbered clock cycles of the bus clock signal and the respective enable signals are output sequentially during all odd-numbered clock signals of the bus clock signal for enabling the respective external circuit elements”.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite in that it fails to point out what is included or excluded by the claim language with the use of the phrase: “**can be**”. This claim is an omnibus type claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 10-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Crouch et al. (U.S. 5,617,531).

As per claim 10, Crouch et al. teaches an integrated circuit comprising all the elements of the instant application. Crouch et al. teaches a plurality of logic gates (201-209) for implementing a logic function of the integrated circuit in Figure 4. Crouch et al. teaches a self-test circuit (Data Processor, 10) that includes a test pattern generator (26) in Figure 1. Crouch et al. teaches a test response analyzer in column 6, lines 26-27, which states: "In BIST mode, the data is sent through the bi-directional bus to the signature analyzer portion of the test controller" (test response analyzer). Crouch et al. teaches an input/output circuit (112, 114, 116) in Figure 3. Crouch et al. teaches a self-test circuit (Data Processor, 10) testing both the plurality of logic gates and the external circuit at the same time in Figure 6. Crouch et al. teaches applying the first part and second part of the test pattern via input/output circuits and the test response being generated in Figure 2.

As per claim 11, Crouch et al. teaches the test pattern generator and the test response analyzer as linear-feedback shifted registers in column 1, line 67 that states: "a PRPG LFSR or Psuedo-Random Pattern Generator Linear Shift Register" and column 3, lines 22-23 that states: "When an LSFR... it is known as a signature analyzer".

Art Unit: 2133

As per claim 12, Crouch et al. teaches a pseudo-random pattern generator in column 1, line 67 through column 3, line 3 that states: "a PRPG LFSR or Psuedo-Random Pattern Generator Linear Shift Register".

As per claims 13 and 14, Crouch et al. teaches an input/output circuit that includes input/output drivers (28 and 29) for sending and receiving unidirectional signals in Figure 1. Crouch et al. also teaches in Figure 1 that these input/output drivers (28 and 29) are controllable (Control Signal, 37).

As per claim 15, Crouch et al. teaches a control device that controls both the self-test circuit and the output circuit that uses a first and second test cycle for testing a plurality of logic gates and the external circuit in column 5, lines 18-27: "processor's single centralized test controller unit"(control device)... "sequence controller selects a next memory after the first memory is tested"(first test cycle) "and repeats the above steps until all memories"(second test cycle for external circuits).

As per claim 16, Crouch et al. teaches a bus connection(Bi-directional Bus, 31) in Figure 1 and a bus control(Bi-directional Control) in Figure 3.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of art with respect to integrated module testing in general:

U.S. Pat No. 5,383,195 to Spence et al.

U.S. Pat No. 5,138,619 to Fasang et al.

U.S. Pat No. 5,737,340 to Tamarapalli et al.

U.S. Pat No. 6,059,451 to Scott et al.

Art Unit: 2133

U.S. Pat No. 5,991,909 to Rajski et al.

U.S. Pat No. 5,748,497 to Scott et al.

U.S. Pat No. 6,148,425 to Bhawmik et al.

U.S. Pat No. 4,835,774 to Ooshima et al.

U.S. Pat No. 6,201,829 to Schneider

U.S. Pat No. 5,574,733 to Kim

U.S. Pat No. 5,383,143 to Crouch et al.

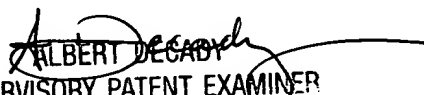
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony T Whittington whose telephone number is 703-306-5617. The examiner can normally be reached on Monday-Friday 7:30a.m.-4:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.



A.W.
May 13, 2003



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